FE1.1s (SSOP28) Layout Guide V2.3

1. All bypass 0.1uF caps, please use size of 0603 and should be as close as possible to the IC(FE1.1s).
2. A 10uF/16V(X5R)/1206 ceramic capacitor, C4, must place near FE1.1s pin 20 (VDD5), also the current path must through the capacitor first before enter the pin 20(VDD5). If the size of 0805 cap must be used, 22uF/6.3V(X5R)/0805 ceramic capacitor preferred.
3. The ground side of 0.1uF cap of FE1.1s pin 28(VD18), must short and efficient connecting to FE1.1s pin 1(VSS), "Add more GND vias(at least 3) near by pin 1(VSS) and ground side of 0.1uF cap", please refer to schematic.
4. DP, DM Differential trace impedance = [DP(45ohm) + DM(45ohm)] = 90 ohm
5. VDD5(pin 20) to VD33_O(pin 21) max current 500mA
6. The DP, DM signal-line should keep 40 mil away from other lines, and the bottom layer should flood with GND (preventing the GND cut).
7. Keep the components out of the XTAL, which also keeping away from DP, DM signals. The bottom layer of XTAL should flood with GND. The shell of XTAL should not connect to the PCB, that will inject the noise to the PCB.
8. The coupling resistor (2.7k+-1%) of the REXT (pin 14) should be as close as possible to the IC, and punch more ground vias at ground side of the resistor.
9. Pin 1 (VSS) is the only GND pin, and should be grounded efficiently, means punching more GND VIAs near by, at least 5 GND vias, as possible.
10. Please refer to the schematic of current path, carefulling the line-width of major current path.
11. The length of 5 couples of DP, DM signal-line, including upstream and all downstream ports, should no less than 1500 mil with 10 of 45-degree-angle, which will degrade the DP DM driving strength in order to pass USB-IF requirement only. If not, the shorter and straighter DP DM signal line, make longer transaction capability (more than 5 meter).
12. Make less jump to the power line. If doing jump of power line,at least 2 of 1mm through holes, need to be drilled. If through holes smaller than 1mm, the number of holes should be doubled.
13. Downstream port's capacitor, 100uF, must as close to each USB connector's Vbus5V as possible.
14. Fuse(2A) need to be low drop type if used.
15. Net of OVCJ and R8 to VCC_5V should be less than 400 mil, leaving far away from any USB connector, and the net's bottom layer should flood with GND (preventing the GND cut), this can prevent the interference of ESD.
16. USB connector's shielding ground should connect to the GND directly without GND cut, and punch more ground vias (15 via/cm^2), this can reduce EMI effect.
17. Adding a Bead/100MHZ/470ohm/2A on Vbus 5V at USB upstream connector could reduce noise from PC(Host).
18. In stead of using power line, the power plane have better stability against to EFT(Electrical Fast Transient).